

Index

- A**
- Address space 20, 21, 23, 34, 62, 116
 - Adversary 28, 31, 36
 - Age 22, 23
 - Aging 23
 - Analysis
 - Average case..... 1
 - Experimental 1, 61
 - Worst-case 1
 - Array..... 34, 35, 49, 55, 56, 57, 58, 59, 67, 72, 74, 80, 95, 99, 100, 107, 108, 109, 110, 113, 115, 116, 121, 131
 - Associative cache..... 18
 - Associativity .18, 19, 21, 24, 25, 30, 32, 84, 114, 123, 132, 135
 - Automatic replacement 32
- B**
- Backward iterator..... 68, 77
 - Basic merger 69
 - Bidirectional iterator 68
 - Binary merge 68
 - Bottom tree 35, 43, 49, 74, 78
 - Branch prediction..... 13, 25, 62, 89, 94
 - Bubblesort..... 55
 - Bucket..... 40, 127
 - Buffer.... 12, 24, 30, 35, 43, 44, 45, 46, 47, 48, 49, 50, 53, 54, 61, 66, 70, 71, 72, 73, 74, 75, 76, 77, 78, 89, 90, 91, 93, 94, 99, 100, 102, 116
 - Buffer, translation look-aside...See Translation Look-aside Buffer
- C**
- C++ programming language 5, 62, 67, 105, 115, 116, 136, 171
 - C++ Programming Language..... 5, 62
 - Cache miss..... 17, 19, 20, 33, 65, 122, 123
 - Categories..... 19
 - Cache-aware 4, 5, 6, 27, 43, 58, 115, 116
 - Cache-oblivious 3, 1, 4, 5, 6, 7, 32, 33, 34, 35, 36, 40, 43, 47, 49, 54, 56, 57, 60, 61, 62, 78, 112, 113, 118, 131, 132, 171
 - CISC See Instruction set
- Computational models..... 1, 4
- Conditional execution 104
 - Conditional move..... 13, 14
 - Conflict cache miss 19
 - Container..... 67
 - Control hazard..... 12
 - CPU time..... 64
- D**
- Data hazard 11
 - Direct mapped 5, 18, 19, 24
 - Direct mapped cache 18
 - Dirty bit 22
 - Distribution sort 40
 - DRAM..... See Memory
- F**
- Flashsort 6
 - Flip 72, 77, 78, 79, 80
 - Forward iterator..... 68, 77
 - Funnel .. 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 66, 67, 71, 72, 73, 74, 76, 77, 78, 79, 80, 83, 84, 88, 89, 91, 97, 99, 100, 102, 103, 107, 108, 109, 110, 111, 112, 116, 124
 - Funnel Heap 47, 50
 - Funnelsort..... 6, 43, 55, 56, 59, 60, 61, 63, 66, 73, 90, 99, 100, 101, 103, 106, 111, 112, 116, 118, 119, 120, 121, 122, 123, 131
- G**
- Generic Algorithms 6
- H**
- Hazard See Pipeline
 - Heapsort 5, 72, 106, 116
- I**
- IA32 instruction set 10
 - Ideal Cache Model 32, 33, 34, 123
 - Inclusion property 19
 - Input iterator..... 68, 77
 - Instruction set

Index

- Complex Instruction Set Computer .10, 11, 14, 20, 24, 62, 104
 - Reduced Instruction Set Computer..10, 11, 13, 14, 16, 20, 24, 25, 62, 104
 - Instruction Set
 - Complex Instruction Set Computer..... 11
 - Reduced Instruction Set Computer..... 11
 - Instruction-level Parallelism..... 11
 - Introsort..... 5, 6
 - IRIX..... 63, 64, 65, 122, 135
 - Iterator..... 67, 68
 - Iterator category..... 67
- K**
- k-merger.....38, 44, 56, 70, 71
- L**
- L1 cache.....19, 20, 25, 84, 95
 - L2 cache 19, 20, 21, 25, 30, 62, 65, 82, 114, 115, 124, 135
 - Latch..... See Pipeline
 - Latency..... 17, 21
 - Lazy funnel.....43, 46, 47, 48
 - Least Recently Used.....18, 22, 23, 25
 - LEDA..... See Library of Efficient Data types and Algorithms
 - LEDA Secondary Memory..... 6, 115
 - LEDA-SM.....LEDA Secondary Memory
 - Library of Efficient Data types and Algorithms..... 6
 - Linux.....23, 63, 64, 65, 116, 135
 - Locality of reference..... 71
 - Locality principle, the..... 17
 - LOWSCOSA..... 7, 56, 57, 59, 60, 61, 108, 109, 111, 112, 116, 118, 119, 120, 121, 123, 127, 131, 132
 - LRU..... See Least Recently Used
- M**
- Magnetic core..... See Memory
 - Manchester design..... Virtual Memory
 - Memory
 - Dynamic Random Access Memory..... 9, 16, 17
 - Magnetic core..... 9, 20
 - Static Random Access Memory..... 9, 16
 - Static Random Access Memory..... 17
 - Virtual..... Virtual Memory
 - Memory Management Unit..... 21, 24
 - Memory mapping..... 23
 - Memory transfer 24, 32, 33, 34, 35, 36, 41, 43, 45, 51, 52, 53, 55, 56, 59, 72, 100, 103, 108, 109, 111, 112, 113, 132
 - Merge tree..... 71, 79
 - Merge tree data structure..... 71, 79
 - Mergesort . 5, 7, 38, 39, 40, 41, 43, 54, 56, 58, 61, 94, 99, 111, 115, 118, 121, 123, 124
 - R-merge..... 5
 - Micro operation..... 11
 - MIPS processor..... 2, 3, 65
 - Miss
 - Capacity..... 19
 - Compulsary..... 19
 - Conflict..... 19, 25, 84, 115, 123
 - MMU..... 21
 - Models
 - Cache-oblivious.....4
 - Computational..... 1
 - External Memory.....4
 - Random Access.....2, 4
- N**
- Navigator..... 73, 76, 77, 78, 79
 - Not Recently Used..... 23
 - NRU..... See Not Recently Used
- O**
- Opteron processor.....20
 - Output iterator..... 68, 77
 - Overlays.....9
- P**
- Page daemon..... 22, 23
 - Page directory..... 21, 22, 24
 - Page fault.....21, 22, 23, 24, 25, 27, 64, 65, 118, 120, 121, 122, 126
 - Page frame..... 20
 - Page frames..... 20, 21
 - Page table..... 21, 22, 23, 24, 30
 - Entry..... 21
 - Pages..... 20, 22, 23, 113, 118, 122
 - PAPI..... See Performance Application Programming Interface
 - Partitioning...31, 40, 41, 59, 105, 108, 109, 110, 111, 112, 116, 124, 128, 130
 - Dutch flag..... 105, 130
 - Performance Application Programming Interface.. 65, 82, 84, 136
 - Physical address..... 21
 - Pipeline. 11, 12, 13, 14, 16, 17, 20, 25, 62, 73, 89, 94, 135
 - Flush..... 13, 17, 89
 - Hazards...11, 12, 13, 15, 16, 17, 20, 25, 62, 73, 87
 - Latch..... 11
 - Stage..... 11
 - Stall..... 12
 - Predication bit..... 13, 104
 - Prediction, branch..... See Branch prediction
- Q**
- Quicksort 5, 6, 40, 41, 55, 63, 103, 108, 109, 112, 116
- R**
- Random access iterator..... 68
 - Referenced bit..... 22, 23, 128
 - Refiller..... 70
 - RISC..... See Instruction set

S

Sets4, 6, 10, 18, 20, 21, 56, 65, 68, 70, 94, 105
 Snooping..... 19
 SRAM..... See Memory
 Stage See Pipeline
 Standard Template Library .. 5, 62, 67, 68, 69, 73, 99,
 101, 105, 116
 Stream... 13, 30, 35, 38, 45, 48, 52, 54, 57, 68, 69, 70,
 72, 76, 88, 89, 90, 91, 93, 95, 96, 97, 111, 116,
 118
 Structural hazard..... 11, 20
 Subarray..... 35

T

TLB See Translation Look-aside Buffer
 Top tree..... 35, 44, 49, 74, 78
 TPIE..... See Transparent Parallel I/O Environment
 TPIE, Transparent Parallel I/O Environment..... 115
 TPIE, Transparent Parallel I/O Environment..... 6
 Translation Look-aside Buffer... 5, 21, 24, 25, 30, 65,
 82, 102, 114, 115, 120, 123, 124, 135

Translation look-aside buffer miss 24, 25, 65, 82, 102,
 120, 123, 124, 135

Tree Operation 54, 72

V

van Emde Boas layout.. 36, 43, 44, 46, 47, 72, 74, 77,
 78, 79, 83, 86, 116

Very Long Instruction Word computer 14

Virtual address 20, 24

Virtual Memory..... 20

VLIW See Very Long Instruction Word computer

W

Wall clock time 1, 64, 65, 103, 118, 124

Windows 63, 64, 65, 116, 136

Write-back..... 10

X

x86 architecture..... 10, 14, 15, 20, 22, 171